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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/755,042	01/09/2004	Mou-Shiung Lin	JCLA8533-D2	8665

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EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/755,042	LIN ET AL.	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *30-40,43-48,52,54-60,139 and 140* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *30-40,43-48,52,54-60,139 and 140* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 30-40, 43, 44, 56, 58, 139 are rejected under 35 U.S.C. 102(e) as being anticipated by Vu et al. (US 2002/0158334 A1).

In re claim 30, Vu (esp. Figs. 3, 10) discloses a semiconductor device, comprising:

a substrate having a surface;

a plurality of dies (section [0030], lines 31-36), wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads located on the active surface, whereas the backside of each die is adhered to the surface of the substrate;

a thin-film circuit layer located over the substrate and the die and having an external circuitry, wherein the external circuitry is electrically connected to the metal pads of the die and extends to a region outside the active surface of the die, the external circuitry has a plurality of bonding pads located on a surface layer of the thin-film circuit layer and each bonding pad is electrically connected to a corresponding metal pad of the die; and

at least one passive device positioned inside or on the thin-film circuit layer, wherein the passive device is selected from a group consisting of an inductor, a wave-guide, a filter, and a micro electronic mechanical sensor (MEMS).

In re claims

In re claim 30, Miura (esp. Fig. 1B, 1C, 1D and 3) discloses a semiconductor device, comprising:

a substrate (36) having a surface;

a plurality of dies (34, 33, 35), wherein each die has an active surface (column 8, lines 16-18), a backside that is opposite to the active surface, and a plurality of metal pads (8) located on the active surface, whereas the backside of each die is adhered to the surface of the substrate (column 8, lines 23-25);

a thin-film circuit layer (9, 21) located over the substrate and the die and having an external circuitry (9a, 9b, 21a, 21b), wherein the external circuitry is electrically connected to the metal pads of the die and extends to a region outside the active surface of the die, the external circuitry has a plurality of bonding pads located on a surface layer of the thin-film circuit layer and each bonding pad is electrically connected to a corresponding metal pad of the die (column 8, lines 29-31, 67; column 9, lines 1-2; and

at least one passive device positioned inside or on the thin-film circuit layer, wherein the passive device is selected from a group an inductor and a filter.[1]

In re claims 31 and 32, Miura discloses the device of claim 30. The limitations, "wherein the dies perform ... functions" are recitations of the intended use of the claimed device. Terms

[1] Inherency dictates the presence of inductors and capacitors (filters) within this structure. Starting with the latter, filters (capacitors) are created in semiconductor technology whenever there are two conductive layers separated by an insulating layer. There are many of such devices in the structure disclosed by Miura. Secondly, parasitic inductors are also formed in devices of this kind. The device of Miura attempts to inhibit this parasitic inductance (column 7, lines 10-15) by shortening the critical path length between chips. A second reference also disclose the build-up of parasitic inductors in these type of devices and the desire to lessen such effect (Arima et al., U.S. Patent No. 5,281,151; column 5, lines 28-35).

that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art.

In re claim 33, Miura discloses the device of claim 30, wherein the dies have an internal circuitry and a plurality of active devices located on the active surface of the die (column 8, lines 25-28), and the internal circuitry is electrically connected to the active devices, whereas the internal circuitry forms the metal pads (column 8, lines 21-23).

In re claim 34, Miura discloses the device of claim 33. The limitation, "wherein a signal ... circuitry" is a recitation of the intended use of the claimed device. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art.

In re claim 35, Miura discloses the device of claim 34, but does not expressly disclose the width, length and thickness of the internal circuitry (column 8, lines 16, 17). Miura discloses a multitude of devices present in the active area (column 8, lines 25-28) and the size of the dies. Of the thousands of semiconductor components present in any given active area, those skilled in the art will recognize that inherency dictates that the width, length, and thickness of the traces of the external circuitry will inherently be greater than that of the traces of the internal circuitry.

In re claim 36, Miura discloses the device of claim 30, wherein the external circuitry further comprises a power/ground bus (column 9, lines 15-18).

In re claim 37, Miura discloses the device of claim 30, wherein the thin-film circuit layer comprises at least a patterned wiring layer (column 10, lines 20-30, 62-67; column 11, lines 1-3) and a dielectric layer (52), the dielectric layer is located over the substrate and the die, and the patterned wiring layer is located over the dielectric layer (Fig. 8), whereas the patterned wiring

layer is electrically connected to the metal pads of the die through the dielectric layer and forms the external circuitry and the bonding pads of the external circuitry.

In re claim 38, Miura discloses the device of claim 37, wherein the dielectric layer has a plurality of thru-holes (16), and the patterned wiring layer is electrically connected to the metal pads of the die via the thru-holes.

In re claim 39, Miura discloses the device of claim 38, wherein a via metal (17; column 8, lines 55-60) is located inside each thru-hole, and the patterned wiring layer is electrically connected to the metal pads of the die by the via metal.

In re claim 40, Miura discloses the device of claim 39, wherein the patterned wiring layer and the via metal form the external circuitry.

In re claim 43, Miura discloses the device of claim 30, wherein the passive device is formed, partly or wholly, by a part of the patterned wiring layer (see Footnote 1).

In re claim 44, Miura discloses the device of claim 37, wherein a material of the dielectric layer is polyimide (column 1, lines 59-60; column 10, lines 25-30).

In re claim 56, Miura discloses the device of claim 30, further comprising a filling layer (36) located between the surface of the substrate and the thin-film circuit layer and surrounding the peripheral of the die, and a surface of the filling layer is planar to the active surface of the die.

In re claim 58, Miura discloses the device of claim 30, further comprising a passivation layer (38) located on top of the thin-film circuit layer and exposing the bond pads (21b).

In re claim 139, Miura discloses the device of claim 30, wherein the substrate further comprises a plurality of inwardly protruded areas (2) located on the surface of the substrate, allowing the dies (4, 5, 6) to be put into the inwardly protruding areas.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 45-48, 52, 59 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over MiurClaims 45-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura as applied to claim 30 above, and further in view of Honda (US 2002/0121689 A1).

In re claims 45 and 59, Miura discloses the device of claim 30, wherein the thin-film circuit layer comprises a plurality of patterned wiring layers and a plurality of dielectric layers, in which the patterned wiring layers and dielectric layers are alternately formed and the patterned wiring layers are electrically connected to the neighboring patterned wiring layers through the dielectric layer, one of the dielectric layers is formed between the thin-film circuit layer and the substrate, the patterned wiring layer that is closest to the substrate is electrically connected to the metal pads of th dies through the dielectric layer that is closest to the substrate. Miura discloses a patterned wiring layer (21b) far away from the substrate and external terminals (20), but does not expressly disclose the external terminals being the farthest away from the substrate. Honda (esp. Fig. 3T) discloses bonding pads (17) attached to patterned wiring layers far away from the

semiconductor substrate (14). It would have been obvious for one skilled in the art at the time of the invention to mount the bonding pads/external terminals/bonding points (claim 59) far away from the substrate as disclosed by Honda for the device of Miura for the purpose, for example, of better facilitating the mounting of the semiconductor device to external semiconductor circuits (Honda; sections [0071 – 0073]).

In re claim 46, Miura in view of Honda discloses the device of claim 45, wherein each of the dielectric layers has a plurality of thru-holes, by which each of the patterned wiring layer is electrically connected to the neighboring patterned wiring layers, where the patterned wiring layer that is closest to the silicon substrate is electrically connected to the metal pads of the dies through the thru-holes that are closest to the substrate.

In re claim 47, Miura in view of Honda discloses the device of claim 46, wherein a via metal is located in each thru-hole, by which the patterned wiring layers are electrically connected to the neighboring patterned wiring layers, where the patterned wiring layer that is closest to the substrate is electrically connected to the metal pads of the die via the via metal that is closest to the substrate.

In re claim 48, Miura in view of Honda discloses the device of claim 47, wherein the patterned wiring layers and the via metal form the external circuitry.

In re claim 52, Miura in view of Honda discloses the device of claim 45, wherein a material of the dielectric layer is polyimide (column 1, lines 59-60; column 10, lines 25-30).

In re claim 60, Miura in view of Honda discloses the device of claim 59, wherein the bonding points are solder balls (Honda; section [0071]).

5. Claim 54 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miura (as above).

In re claim 54, Miura discloses the device of claim 30, wherein the substrate (3) comprises ceramic (a heat conducting layer) formed overlapping (Fig. 1A) the surface of the substrate provided by a surface of the heat conducting layer, the substrate has a plurality of openings (2) that penetrate through the layer to form the inwardly protruded areas, allowing the dies put into the inwardly protruding areas. Miura also discloses the use of silicon as a material for the substrate, but not the two in combination. Silicon is also the material of choice for the dies (4, 5, 6). It would have been obvious for one skilled in the art at the time of the invention to surround the silicon LSI regions of Miura with a ceramic material as disclosed by Miura for the purpose, for example, of helping to dissipate heat during the operation of the device.

6. Claims 55 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura as applied to claim 54 above, and further in view of Vu et al. (US 2002/0158334 A1).

In re claim 55, Miura discloses the device of claim 54, but does not expressly disclose the thickness of the substrate layer being approximately equal to a thickness of the dies. Vu (esp. Fig. 10) discloses the thickness of the substrate layer (36) being approximately equal to a thickness of the dies (10). It would have been obvious for one skilled in the art at the time of the invention to use the thinner substrate design as disclosed by Vu for the device of Miura for the purpose, for example, of reducing the metallization pitch to be used on successive build up layers (Vu; section [0019]).

In re claim 57, Miura discloses the device of claim 56, but does not expressly disclose a material of the filling layer consisting of epoxy or polymer. Vu (Fig. 10) discloses a filling layer

(38) comprising a polymer such as epoxy (section [0017], lines 9-10). It would have been obvious for one skilled in the art at the time of the invention to use an encapsulant as disclosed by Vu for the device of Miura for the purpose, for example, of providing better insulation between active regions.

7. Claim 140 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miura as applied to claim 139 above, and further in view of Shanefield (U.S. Patent No. 4,866,501).

In re claim 140, Miura discloses the device of claim 139, but does not expressly disclose the substrate comprising silicon. Shanefield (esp. Fig 1) discloses a substrate a comprising silicon wafer (10). It would have been obvious for one skilled in the art at the time of the invention to use a silicon wafer as disclosed by Shanefield for the device of Miura for the purpose, for example, of better facilitation cutting of the device into dies.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty
Examiner
Art Unit 2815